said at least one MOS transistor includes:

a first MOS transistor being formed on said depressed region, and

a second MOS transistor being formed on said ordinary region, and

cont. B1 a length of a margin part of a first gate electrode constructing said first MOS transistor in said depressed region is set to be larger than that of a margin part of a second gate electrode constructing said second MOS transistor in said ordinary region, wherein a length of the margin part of the second gate electrode is X, the length of the margin part of the first gate electrode is $X \neq \alpha$ where $0 < \alpha \leq X$.

12. (Amended) A method of fabricating a semiconductor device on the basis of a layout design, the layout design achieved by a process comprising the steps of:

B2 designing a layout of an active area on a plane, said active area being defined from an insulating film by a boundary including a first edge extending along a first direction and a second edge extending along the first direction and a third edge connected between one ends of the first and second edges extending along a second direction different from the first direction, said first to third edges forming a step shape so that the second edge is depressed toward an inside of said active area beyond the first edge;

designing a layout of a first gate electrode of a first MOS transistor on said active area, one end of said first gate electrode extending to an outside of said active area across the first edge in a vertical direction to the first direction, and